SPECIFICATION AMENDMENTS

Please replace the paragraph beginning at page 1, line 12, with the following amended paragraph:

The invention relates to a frequency-stabilized transceiver configuration which is intended to be used in communication terminals for wire-connected and/or wireless communication. The transceiver configuration ~~enfiguration~~ has an A/D converter outputting ~~outputing~~ a first digital data signal, a D/A converter, and a controllable oscillator circuit. The controllable oscillator ~~oscialloctor~~ circuit has a reference oscillator with an oscillating crystal as a resonator and outputs a sampling clock received by the A/D converter and the D/A converter. A digital data processing circuit receives the first digital data signal output by the A/D converter and processes it further and outputs a second digital data signal to the D/A converter. A frequency section being a radio-frequency and/or an intermediate-frequency section is provided and has a frequency converter stage operated with a beat frequency derived from the controllable oscillator circuit.

Please replace the paragraph beginning at page 2, line 8, with the following amended paragraph:

A central variable in the transmission of messages is the bandwidth available for transmission since it limits the maximum achievable number of messages which can be transmitted per unit time when a minimum transmission quality is stipulated. As a rule, the available bandwidth ~~bandwidths~~ is limited. Apart from software approaches to the bandwidth problem which are also based on stipulating a suitable data structure, the best-possible utilization of the available bandwidth must also always be ensured on the hardware side.

Please replace the paragraph bridging page 4 and page 5, beginning at page 4, line 22, with the following amended paragraph:

With the foregoing and other objects in view there is provided, in accordance with the invention, a transceiver configuration for a communication terminal. The transceiver configuration contains an A/D converter outputting ~~outputing~~ a first digital data signal, a D/A converter and a controllable oscillator circuit connected to the A/D converter and to the D/A converter. The controllable oscillator ~~oscialloetor~~ circuit has a reference oscillator with an oscillating crystal as a resonator and outputs a sampling clock received by the A/D converter and the D/A converter. A digital data processing circuit is connected to

the A/D converter and to the D/A converter and receives the first digital data signal output by the A/D converter and processes it further and outputs a second digital data signal to the D/A converter. The A/D converter, the D/A converter, the data processing circuit and the controllable oscillator circuit, apart from the oscillating crystal of the reference oscillator, are constructed as a monolithically integrated circuit so that of the controllable oscillator circuit, only the oscillating crystal is implemented as an external component. A frequency section being a radio-frequency section and/or an intermediate-frequency section is connected to the A/D converter, to the D/A converter and to the controllable oscillator circuit. The frequency section has a frequency converter stage operating with a beat frequency derived from the controllable oscillator circuit.

Please replace the paragraph beginning at page 7, line 12, with the following amended paragraph:

Fig. 1 is a block <u>circuit</u> ~~eireiut~~ diagram of a circuit configuration according to the invention;